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EXAMINER	
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2112	12

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/490,132	Applicant(s) MOYER, WILLIAM C.	
	Examiner Kim T. Huynh	Art Unit 2112	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6,8-17 and 19-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *14-16 and 22* is/are allowed.

6)☒ Claim(s) *1-5,8-13,17 and 19-21* is/are rejected.

7)☒ Claim(s) *6* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 January 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1, 3-5 and 8, 19-21 are rejected under 35 U.S.C. 102(e) as being anticipated by Arndt et al. (US Patent 5,701,495)

As per claims 1, 8, Arndt discloses a method for implementing interrupts in a data processing system, comprising the steps of:

- providing a first storage device (fig.5, 56) having a plurality of inputs , each of the plurality of inputs (interrupt signals) being coupled by a respective physical conductor to one of a plurality of hardware-generated interrupt sources (col.7, lines 6-13) which selectively generate hardware interrupts and selectively storing the hardware interrupts, the first storage device providing one or more hardware-generated interrupt signals. *[(note, storage queue (56) comprises plurality of hardware interrupts which generated by I/O controller (fig.2, 34) , (col.4, lines 25-52), (col.8, lines 56-67), wherein interrupt signals associated with a particular processor implies interrupt signals associated with physical conductor*]

- providing a second storage device (fig.5, 57) having one or more inputs, each of the one or more inputs (means interrupt signals) receiving and storing a predetermined one of a plurality of software-generated interrupt signals, at least some of the predetermined plurality of software-generated interrupt signals indicating an interrupt from a different source or of a different type than the hardware interrupts, the second storage device providing one or more software-generated interrupt signals. [*(col.9, lines 1-5), (col.8, lines 6-12), wherein queue 57 comprises plurality of software and hardware interrupts signals which can be specified by value of external interrupt source register), (col.18, lines 20-27), (col.2, lines 19-43)*
- coupling logic circuitry (fig.5, 55) to the first storage device and the second storage device for receiving the one or more hardware-generated interrupt signals and the one or more software-generated signals, the logic circuitry providing an interrupt request signal which will cause an interrupt to occur in the data processing system. *[(fig.5, 55 queues wherein receiving and selecting plurality of interrupts types from the hardware and software queues in 56 and 57, (col.8, lines 62-65), (col.9, lines 1-6)]*
- a plurality of hardware interrupt sources *[(fig.5, 56); (col.7, lines 7-21)]*
- executing software with the data processing system to generate a predetermined software-generated interrupt signal which emulates a predetermined one of the hardware-generated interrupt sources

but with a priority which differs from the predetermined one of the hardware-generated interrupt sources, thereby dynamically changing prioritization of servicing of interrupts in the data processing system; *[(col.10, lines 1-23), (col.9, lines 55-67), (col.12, lines 56-65), note, an assigned value interrupt is signaled to processor by the hardware via interrupt signal into the processor hardware, then the software receive and read and store this value once this interrupt has been presented this will signals hardware that software will start processing this implies emulation ,furthermore, software sets and removes priority which implies changing prioritization of servicing.)]*

- assigning an interrupt prioritization level to each of a plurality of storage locations of the first storage device and to each of a plurality of storage locations of the second storage device. (*fig.3, col.4, lines 25-31, wherein prioritized list of events implies prioritization level of a plurality of storage locations.)*

As per claims 3 and 19, Arndt discloses a method further comprising the step of assigning a portion of the plurality of software-generated interrupt signals stored in the second storage device to represent interrupts from some interrupt sources generating hardware interrupt and having a corresponding interrupt prioritization level *[(col.4, lines 25-32), note from fig.5, 55 step of selecting the priority between hardware and software interrupts from fig.2, 42&43 storage queues comprise list of prioritized list of events associated with a logical server)]*

As per claims 4 and 20, Arndt discloses a method further comprising the step of assigning a portion of the plurality of software-generated interrupt signals stored

in the second storage device to represent interrupts from same interrupt sources generating hardware interrupts and having an interrupt prioritization level which differs from the interrupt prioritization level of the plurality of hardware-generated interrupt sources coupled to the first storage device *[(col.4, lines 1-67), note from fig.5,55 step of selecting priority between hardware and software interrupts from fig.2, 42&43 storage queues comprise list of prioritized list of events; events are from external interrupts from IOC and inter-processor interrupts)]*

As per claims 5 and 21, Arndt discloses method further comprising the step of changing interrupt servicing from servicing a hardware-generated interrupt and switching to servicing a software-generated interrupt of higher prioritization before completion of servicing of the hardware-generated interrupt occurs. *[(col.10, lines 12-23) (note, software remove and sets what interrupt servicing routing to revoke, (col.6, lines 45-63), changing operation priority implies changing interrupts services)]*

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Arndt et al (US Patent 5,701,495) in view of Simpson et al. (US Patent 6,185,629)

As per claim 2, Arndt discloses all the limitations as above except the limitation that determining priority between two interrupts, a first interrupt being hardware-generated and a second interrupt being software-generated, when the two

interrupts have a same prioritization level by choosing to service one of the hardware-generated first interrupt or the software-generated second interrupt. However, Simpson discloses determining priority for multiple requests from different processors of the same priority, it will form a round robin between them round robin will always be passed to the next processor with a pending request in the chain, this prevents requests of equal priority from other processors need to be serviced. (col.25, lines 17-27)

It would have been obvious one having ordinary skills in the art at the time the invention was made to incorporate Simpson's teaching into Arndt's method to include the round robin for determining the priority between the same prioritization level between software and hardware so as to be advanced avoiding interrupts suspended due to time-out fault or error. (col.72, lines 55-67)

5. Claims 9, 11-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Arndt et al (US Patent 5,701,495) in view of Simpson et al. (US Patent 6,185,629), and further in view of Donovan (US Patent 5,987,601)

As per claim 9 Arndt discloses:

- providing a first storage device (fig.5, 56) having a plurality of inputs , each of the plurality of inputs (interrupt signals) being coupled by a respective physical conductor to one of a plurality of hardware-generated interrupt sources (col.7, lines 6-13) which selectively generate hardware interrupts and selectively storing the hardware interrupts, the first storage device providing one or more

hardware-generated interrupt signals. *[(note, storage queue (56) comprises plurality of hardware interrupts which generated by I/O controller (fig.2, 34) , (col.4, lines 25-52), (col.8, lines 56-67), wherein interrupt signals associated with a particular processor implies interrupt signals associated with physical conductor*]

- providing a second storage device (fig.5, 57) having one or more inputs, each of the one or more inputs (means interrupt signals) receiving and storing a predetermined one of a plurality of software-generated interrupt signals, at least some of the predetermined plurality of software-generated interrupt signals indicating an interrupt from a different source or of a different type than the hardware interrupts, the second storage device providing one or more software-generated interrupt signals. [*(col.9, lines 1-5), (col.8, lines 6-12), wherein queue 57 comprises plurality of software and hardware interrupts signals which can be specified by value of external interrupt source register), (col.18, lines 20-27), (col.2, lines 19-43)*
- coupling logic circuitry (fig.5, 55) to the first storage device and the second storage device for receiving the one or more hardware-generated interrupt signals and the one or more software-generated signals, the logic circuitry providing an interrupt request signal which will cause an interrupt to occur in the data processing system. *[(fig.5, 55 queues wherein receiving and selecting plurality of interrupts types from the hardware and software queues in 56 and 57, (col.8, lines 62-65), (col.9, lines 1-6)]*

- a plurality of hardware interrupt sources *[(fig.5, 56); (col.7, lines 7-21)]*
- executing software with the data processing system to generate a predetermined software-generated interrupt signal which emulates a predetermined one of the hardware-generated interrupt sources but with a priority which differs from the predetermined one of the hardware-generated interrupt sources, thereby dynamically changing prioritization of servicing of interrupts in the data processing system; *[(col.10, lines 1-23), (col.9, lines 55-67), (col.12, lines 56-65), note, an assigned value interrupt is signaled to processor by the hardware via interrupt signal into the processor hardware, then the software receive and read and store this value once this interrupt has been presented this will signals hardware that software will start processing this implies emulation ,furthermore, software sets and removes priority which implies changing prioritization of servicing.)]*
- wherein the hardware interrupt storage device and the software interrupt storage device have an assigned interrupt prioritization level to specific storage locations(*fig.3, col.4, lines 25-31*), assignment of the interrupt prioritization level of the interrupt sources associated with the software-generated interrupt signals being variable by software control. (*col.10, lines 19-22, col.9, lines 16-25),note the software removes and sets priority in the queue*)

Arndt discloses all the limitations as above except the limitation that determining priority between two interrupts, a first interrupt being

hardware-generated and a second interrupt being software-generated, when the two interrupts have a same prioritization level by choosing to service one of the hardware-generated first interrupt or the software-generated second interrupt. However, Simpson discloses determining priority for multiple requests from different processors of the same priority, it will form a round robin between them round robin will always be passed to the next processor with a pending request in the chain, this prevents requests of equal priority from other processors need to be serviced. (col.25, lines 17-27)

It would have been obvious one having ordinary skills in the art at the time the invention was made to incorporate Simpson's teaching into Arndt's method to include the round robin for determining the priority between the same prioritization level between software and hardware so as to be advanced avoiding interrupts suspended due to time-out fault or error. (col.72, lines 55-67) and

Further regarding to the interrupt prioritization level of the hardware interrupt sources being permanently assigned limitation. Donavan discloses the major interrupt sources is assigned a fixed hardware task number. *(col.5, lines 57-62)*

It would have been obvious to one having ordinary skills in the art at the time the invention was made to incorporate Donavan's teaching into the modified of Arndt's system to have the hardware

interrupt source being permanently assigned so as to limiting the number of tasks change in the system. *(col.2, lines 16-22)*

As per claim 11, Arndt discloses a software-generated interrupt signal of higher priority than a currently executing hardware-generated interrupt signal is provided to the logic circuitry prior to completion of an associated hardware interrupt servicing, and the data processing system suspends processing of the hardware interrupt servicing to process an associated software interrupt servicing. *(col.6, lines 45-63)*

As per claim 12, Arndt discloses a mask register coupled to the hardware interrupt storage device and the software interrupt storage device for selectively preventing hardware-generated interrupt signals and software-generated interrupt signals from propagating to the logic circuitry. *(col.12, lines 10-31)*

As per claim 13, Arndt discloses the hardware interrupt storage device and the software interrupt storage device are each implemented as latch circuits *[(fig.1, 34) note, interrupt signals control and configure by controller (fig.2, 34), (col.4, lines 17-24)]*

6. Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Arndt et al. (US Patent 5,701,495) in view of Donovan (US Patent 5,987,601)

Arndt discloses wherein the hardware interrupt storage device and the software interrupt storage device have an assigned interrupt prioritization level to specific storage locations, (*fig.3, col.4, lines 25-31*) assignment of the interrupt prioritization level of the interrupt sources associated with the software-generated interrupt signals being variable by software control. (*col.10, lines 19-22, col.9, lines 16-25),note the software removes and sets priority in the queue*)

Arndt discloses all the limitation as above except the limitation that the interrupt prioritization level of the hardware interrupt sources being permanently assigned. However, Donavan discloses the major interrupt sources is assigned a fixed hardware task number. *(col.5, lines 57-62)*

It would have been obvious to one having ordinary skills in the art at the time the invention was made to incorporate Donavan's teaching into Arndt's method to have the hardware interrupt source being permanently assigned so as to limiting the number of tasks change in the system. *(col.2, lines 16-22)*

CLAIMS OBJECTION

7. Claim 6 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Prior art does not teach or suggest the step of changing prioritization level of a predetermined hardware-generated interrupt by providing a software-generated interrupt which represents a corresponding hardware-generated interrupt source for the predetermined hardware-generated interrupt but with a different prioritization level than the predetermined hardware-generated interrupt.

Allowable Subject Matter

8. Claims 14-16, 22 are allowable.

Response to Arguments

9. Applicant's arguments filed on 3/09/04 have been considered but does not place application in condition for allowance.

a. Applicant argues that Arndt does not disclose assigning an interrupt prioritization level to each of a plurality of storage locations of the first storage device and to each of a plurality of storage locations of the second storage device. Examiner respectively disagrees. As Arndt notes at (*fig.3, col.4, lines 25-31*) the logical view of the system as seen from the system software is that of n (up to 256) queues of events. Within each software queue there exists a prioritized list of events (interrupt prioritization level). These events comprise hardware generated interrupts and software generated interrupts, wherein prioritized list of events implies prioritization level of a plurality of storage locations. Thus, the prior art teaches the invention as claimed and the amended claims do not distinguish over the prior art as applied.

Conclusion

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kim Huynh whose telephone number is (703)305-5384 or via e-mail addressed to [kim.huynh3@uspto.gov]. The examiner can normally be reached on M-F 8:30AM- 6:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Rinehart can be reached on (703) 305-4815 or via e-mail addressed to [mark.rinehart@uspto.gov]. The fax phone numbers for the organization where this application or proceeding is assigned are (703)872-9306 for regular communications and After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)306-5631.

Kim Huynh

March 30, 2004

Khanh Dang
Primary Examiner